What is claimed is:

1. A nonvolatile memory comprising:

a memory array unit having a plurality of nonvolatile memory cells; a control unit; and a voltage generating unit for supplying voltages to said nonvolatile memory cells,

wherein said nonvolatile memory cells store information corresponding to the quantity of electric charges in a floating gate of each nonvolatile memory cell,

wherein said control unit controls a write operation to store information into said nonvolatile memory cells; a read operation to read information stored in said nonvolatile memory cells; and an erase operation to erase information stored in said nonvolatile memory cells,

wherein said voltage generating unit has an erase voltage generating unit for generating, in accordance with control from said control unit, erase voltages to be applied to said nonvolatile memory cells in said erase operation, and

wherein said erase voltage generating unit generates, on the basis of a control signal supplied from said control unit, erase voltages of two or more levels and applying them to a control gate of each of said nonvolatile memory cells.

2. A nonvolatile memory comprising:

a memory array unit having a plurality of nonvolatile memory cells; a control unit; and a voltage generating unit for supplying voltages to said nonvolatile memory cells,

wherein said nonvolatile memory cells store information corresponding to the quantity of electric charges in a floating gate of each nonvolatile memory cell,

wherein said control unit controls a write operation to store information into said nonvolatile memory cells; a read operation to read information stored in said nonvolatile memory cells; and an erase operation to erase information stored in said nonvolatile memory cells,

wherein said voltage generating unit has an erase voltage generating unit for generating, in accordance with control from said control unit, erase voltages to be applied to said nonvolatile memory cells in said erase operation, and

wherein said erase voltage generating unit generates, on the basis of a control signal supplied from said control unit, erase voltages of two or more levels to make the voltages applied to the tunnel films of said nonvolatile memory cells substantially constant and applies them to a control gate of each of said nonvolatile memory cells.

3. The nonvolatile memory according to Claim 2, wherein said erase voltage generating unit, after applying erase voltages of two or more different levels to said control gates of said nonvolatile memory cells, verifies the erase.

4. The nonvolatile memory according to Claim 3, wherein, out of the erase voltages generated by said erase voltage generating unit, a first voltage level of an erase voltage first

applied to said control gate of any of said nonvolatile memory cell is the lowest, and each of the erase voltages applied second and afterwards is higher in level than the erase voltage applied immediately before.

5. A data erasing method for a nonvolatile memory having a plurality of nonvolatile memory cells which store information corresponding to the quantity of electric charges in a floating gate of each nonvolatile memory cell,

wherein an operation to erase data in said nonvolatile memory cells is performed by applying an erase voltage, while being switched between two or more different levels, to a control gate of each of said nonvolatile memory cells, and

wherein no erase verification is performed in said erase operation until said erase voltage of two or more levels is applied to said nonvolatile memory cells.

6. A data erasing method for a nonvolatile memory having nonvolatile memory cells which store information corresponding to the quantity of electric charges in a floating gate of each nonvolatile memory cell,

wherein erase voltages of two or more levels to make the voltages applied to the tunnel films of said nonvolatile memory cells substantially constant are applied, while being changed between two or more different levels, to a control gate of each of said nonvolatile memory cells to erase data in said nonvolatile memory cells, and

wherein no erase verification is performed in said erase operation until said erase voltage of two or more levels is applied to all the cells.

7. The data erasion method for a nonvolatile memory according to Claim 6, wherein, out of the erase voltages, a first erase voltage first applied to the control gate of any of the nonvolatile memory cell is the lowest in the voltage level, and each of the erase voltages changed to the second time and afterwards is higher in the level than the erase voltage applied immediately before.

8. A nonvolatile memory comprising, on one semiconductor substrate, a memory array unit; a control unit; and a voltage generating unit,

wherein said memory array unit has a plurality of word lines and a plurality of nonvolatile memory cells,

wherein each of the nonvolatile memory cells has a first terminal connected to a first semiconductor region; a second terminal connected to a second semiconductor region; and a third terminal connected to a control gate;

wherein there is an electric charge accumulating region above a channel region between said first semiconductor region and said second semiconductor region and between it and said control gate; and there is a first insulating film between the electric charge accumulating region and the channel region,

wherein the third terminal of at least one nonvolatile

memory cell is connected to each word line,

wherein data are stored into each nonvolatile memory cell according to the quantity of electric charges accumulated in said electric charge accumulating region; and the quantity of electric charges is controlled by the control of said control unit over a first operation to inject electric charges into said electric charge accumulating region and a second operation to eject electric charges out of said electric charge accumulating region,

wherein, in order to perform said second operation, a voltage generated by said voltage generating unit is applied between said control gate and channel region via a word line connected to the control gate, and

wherein, during the period of said second operation, the voltage generated by said voltage generating unit is varied twice or more, so as to keep the voltage applied to said first insulating film within a predetermined voltage range.

9. The nonvolatile memory according to Claim 8,

wherein, during said first operation, the voltage generated by said voltage generating unit is applied between said control gate and channel region via a word line connected to the control gate, and

wherein, during said first operation, the voltage generated by said voltage generating unit is varied.

10. The nonvolatile memory according to Claim 9,

wherein, the voltage applied between said control gate and

channel region in said first operation differs in polarity from the voltage applied between said control gate and channel region in said second operation.

11. The nonvolatile memory according to Claim 10,

wherein the threshold voltage of the nonvolatile memory cells is varied according to the quantity of electric charges accumulated in said electric charge accumulating region so as to be included in a plurality of threshold voltage distributions according to data to be stored into said nonvolatile memory cells,

wherein in said first operation, the threshold voltage of the nonvolatile memory cells are moved into a first threshold voltage distribution, and a first determination is made during said first operation as to whether or not the threshold voltage of the nonvolatile memory cells are moved within said first threshold voltage distribution,

wherein in said second operation, the threshold voltage of the nonvolatile memory cells are moved into a second threshold voltage distribution; and a second determination is made during said second operation as to whether or not the threshold voltage of the nonvolatile memory cells are moved within said second threshold voltage distribution,

wherein said threshold voltage of at least one of a plurality of nonvolatile memory cells connected to one word line is moved, in said first operation, and

wherein said threshold voltages of all of the plural

nonvolatile memory cells connected to one word line are moved, in said second operation.